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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,676	02/04/2002	Morteza Hagh-Panah	PA1949US	8787

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 01/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/068,676	HAGH-PANAH ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date: _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, claims 1-5, in the reply filed on 07/12/2004 is acknowledged.

Specification

2. The disclosure is objected to because of the following informalities: Claims 1-5 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. A description of what a multiple cyclic redundancy check circuit critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). The Applicant uses the term multiple byte-wise CRC circuit in various places throughout the specification, but nowhere in the Application doe the Applicant teach what a multiple cyclic redundancy check circuit is.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-5 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. A description of what a multiple cyclic redundancy check circuit critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). The Applicant uses the term multiple byte-wise CRC circuit in various places throughout the specification, but nowhere in the Application doe the Applicant teach what a multiple cyclic redundancy check circuit is.

Claims 1-5 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 1 recites, "A method of performing a cyclic redundancy check calculation on a data stream composed of segments of data, comprising: **providing** multiple cyclic redundancy check circuits, at least one cyclic redundancy check circuit able to perform the cyclic redundancy check calculation on a maximum amount of data and at least one cyclic redundancy check circuit able to perform the cyclic redundancy check calculation on a minimum amount of data, each cyclic redundancy check circuit capable of using prior cyclic redundancy check calculation results" [Emphasis added]. Nowhere in the specification does the Applicant teach a step for **providing** multiple cyclic redundancy check circuits as part of a method of performing a cyclic redundancy check calculation (Note: the step for **providing** multiple cyclic redundancy check circuits is generally a

design and manufacture step whereby check circuits are designed and built onto circuitry for providing error protection).

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "multiple cyclic redundancy check circuits" is indefinite since it can have mor then one meaning: 1) a plurality of cyclic redundancy check circuits whereby one cyclic redundancy check circuit is a unit element in the plurality of elements or 2) a plurality of multiple cyclic redundancy check circuits whereby one multiple cyclic redundancy check circuit is a unit element in the plurality of elements.

Claim 1 recites the limitation "the cyclic redundancy check calculation" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 1 recites the limitation "the cyclic redundancy check calculation" in line 6. There is insufficient antecedent basis for this limitation in the claim.

The term "maximum amount of data" in claim 1 is a relative term which renders the claim indefinite. The term "maximum amount of data" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the

invention. The maximum amount of data can be any number and in fact does not have to be different from the minimum amount of data.

The term "minimum amount of data" in claim 1 is a relative term which renders the claim indefinite. The term "minimum amount of data" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The minimum amount of data can be any number and in fact does not have to be different from the maximum amount of data.

Claim 1 recites the limitation "the appropriate cyclic redundancy check circuit" in lines 11-12. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 recites, "the multiple cyclic redundancy check circuits includes: an eight byte cyclic redundancy check circuit; a seven byte cyclic redundancy check circuit; a six byte cyclic redundancy check circuit; a five byte cyclic redundancy check circuit; a four byte cyclic redundancy check circuit; a three byte cyclic redundancy check circuit; a two byte cyclic redundancy check circuit; and a single byte cyclic redundancy check circuit." The Examiner asserts that whether 1) each multiple cyclic redundancy check circuit includes: an eight byte cyclic redundancy check circuit; a seven byte cyclic redundancy check circuit; a six byte cyclic redundancy check circuit; a five byte cyclic redundancy check circuit; a four byte cyclic redundancy check circuit; a three byte cyclic redundancy check circuit; a two byte cyclic redundancy check circuit; and a single byte cyclic redundancy check circuit or 2) whether the eight byte cyclic redundancy check circuit; the seven byte cyclic redundancy check circuit; the six byte cyclic redundancy check

circuit; the five byte cyclic redundancy check circuit; the four byte cyclic redundancy check circuit; the three byte cyclic redundancy check circuit; the two byte cyclic redundancy check circuit; and the single byte cyclic redundancy check circuit are distributed in another fashion amongst the multiple cyclic redundancy check circuits. Claim 5 recites the limitation "the cyclic redundancy check calculation" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Claim 1 recites, "providing multiple cyclic redundancy check circuits, at least one cyclic redundancy check circuit able to perform the cyclic redundancy check calculation". The omitted structural cooperative relationships are: the relationships between a multiple cyclic redundancy check circuit, the multiple cyclic redundancy check circuits and the at least one cyclic redundancy check circuit.
Claim 1 recites, "at least one cyclic redundancy check circuit able to perform the cyclic redundancy check calculation on a maximum amount of data and at least one cyclic redundancy check circuit able to perform the cyclic redundancy check calculation on a minimum amount of data". The omitted structural cooperative relationships are: the relationships between "a maximum amount of data" and "a minimum amount of data" (Note: as stated the maximum amount of data may be equal to the minimum amount of data). The omitted structural cooperative relationships are: the relationships between

"the cyclic redundancy check calculation on a maximum amount of data" and "the cyclic redundancy check calculation on a minimum amount of data".

Claim 1 recites, "processing the segment of data with the appropriate cyclic redundancy check circuit". The omitted structural cooperative relationships are: the relationships between "multiple cyclic redundancy check circuits" and "the appropriate cyclic redundancy check circuit". The omitted structural cooperative relationships are: the relationships between "multiple cyclic redundancy check circuits" and a "cyclic redundancy check circuit".

Claim 4 recites, "the multiple cyclic redundancy check circuits includes: an eight byte cyclic redundancy check circuit; a seven byte cyclic redundancy check circuit; a six byte cyclic redundancy check circuit; a five byte cyclic redundancy check circuit; a four byte cyclic redundancy check circuit; a three byte cyclic redundancy check circuit; a two byte cyclic redundancy check circuit; and a single byte cyclic redundancy check circuit." The omitted structural cooperative relationships are: the relationships between a "multiple cyclic redundancy check circuit" and "a seven byte cyclic redundancy check circuit; a six byte cyclic redundancy check circuit; a five byte cyclic redundancy check circuit; a four byte cyclic redundancy check circuit; a three byte cyclic redundancy check circuit; a two byte cyclic redundancy check circuit; and a single byte cyclic redundancy check circuit".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Hyodo; Ryuji et al. (US 5282215 A, hereafter referred to as Hyodo).

35 U.S.C. 102(b) rejection of claim 1.

Hyodo teaches providing multiple cyclic redundancy check circuits (EX-OR circuits receiving α_3, α_4,..., α_{p+1} bits in Figure 3 of Hyodo are multiple cyclic redundancy check circuits), at least one cyclic redundancy check circuit able to perform the cyclic redundancy check calculation on a maximum amount of data (one of α_3, α_4,..., α_{p+1} in Figure 3 of Hyodo is a maximum; hence at least one cyclic redundancy EX-OR check circuit is able to perform the cyclic redundancy check calculation on a maximum amount of data; Note: even if all of α_3, α_4,..., α_{p+1} are equal a maximum still exists and is equal to the minimum) and at least one cyclic redundancy check circuit able to perform the cyclic redundancy check calculation on a minimum amount of data (one of α_3, α_4,..., α_{p+1} in Figure 3 of Hyodo is a minimum; hence at least one cyclic redundancy EX-OR check circuit is able to perform the cyclic redundancy check calculation on a minimum amount of data; Note: even if all of α_3, α_4,..., α_{p+1} are equal a minimum still exists and is equal to the maximum), each cyclic redundancy check circuit capable of using prior cyclic

redundancy check calculation results (each cyclic redundancy EX-OR check circuit receiving $\alpha_3, \alpha_4,\ldots, \alpha_{p+1}$ bits in Figure 3 of Hyodo is capable of using prior cyclic redundancy check calculation results); determining which of the multiple cyclic redundancy check circuits is appropriate for the segment of data to be processed (Figure 6 in Hyodo teaches a means for determining which of the multiple cyclic redundancy check circuits is appropriate for the segment of data to be processed); processing the segment of data with the appropriate cyclic redundancy check circuit (Figure 3 in Hyodo teaches a means for processing the segment of data with the appropriate cyclic redundancy check circuit); and repeating the steps of determining which redundancy check circuit is appropriate and processing the segment of data with the appropriate cyclic redundancy check circuit until there are no more segments of data to process (the Abstract in Hyodo teaches that the CRC calculations are carried out continuously on the headers in the ATM cells; hence the steps of determining which redundancy check circuit is appropriate and processing the segment of data with the appropriate cyclic redundancy check circuit until there are no more segments of data to process are repeated continuously as the transmission system continues to receive data).

35 U.S.C. 102(b) rejection of claim 3.

$\alpha_3, \alpha_4,\ldots, \alpha_{p+1}$ bits in Figure 3 of Hyodo are variables; hence the teachings in Hyodo encompass $\max(\alpha_3, \alpha_4,\ldots, \alpha_{p+1}) = 8$ bytes.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hyodo; Ryuji et al. (US 5282215 A, hereafter referred to as Hyodo) in view of Moon; Bong-Chae et al. (US 6675236 B2, hereafter referred to as Moon).

35 U.S.C. 103(a) rejection of claim 2.

Hyodo substantially teaches the claimed invention described in claim 1 (as rejected above).

However Hyodo does not explicitly teach the specific use of an interface board.

Moon, in an analogous art, teaches use of an interface board (see interface board in Figure 1 of Moon).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hyodo with the teachings of Moon by including use of an interface board. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of an interface board would have provided the opportunity to provide error protection in a digital communication system.

7. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hyodo; Ryuji et al. (US 5282215 A, hereafter referred to as Hyodo) in view of Kimmitt; Myles (US 6530057 B1).

35 U.S.C. 103(a) rejection of claims 4 and 5.

Hyodo substantially teaches the claimed invention described in claim 1 (as rejected above).

However Hyodo does not explicitly teach the specific use of the various sized CRC circuits.

Kimmitt, in an analogous art, teaches use of the various sized CRC circuits (see Figure 7-11 in Kimmit).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hyodo with the teachings of Kimmitt by including use of the various sized CRC circuits. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill

in the art would have recognized that use of the various sized CRC circuits would have provided the opportunity for unequal error protection.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133